transistor Q16 and the bases of the transistors Q17 and Q18 are connected to the base of transistors Q15, no collector current flows to the transistor Q16 because a voltage between base and emitter is 0V. Therefore, the IREF is equal to the sum of the collector current of the transistors Q17 and Q18; namely becomes $2 \cdot I7$.

As described above, by controlling the switches S1 and S2, the variable current source 7 can output two kinds of IREF having a current value of 1:2.

According to this first embodiment, the variable-gain phase comparator 1 capable of varying a phase difference conversion gain is used as a phase comparator of the PLL circuit, and thereby, only one VCO is operated in accordance with a desired operation frequency band. Moreover, the phase difference conversion gain is varied in accordance with the sensitivity of the VCOs 4-1 to 4-n, and thereby, the number of LPF 3 required for the PLL circuit can be reduced to only one. Therefore, it is possible to reduce the number of pins of IC in which the phase comparator is built, and thus, to simplify a design of the PLL circuit.

(Embodiment 2)

Next, the following is a description on a PLL circuit according to a second embodiment of the present invention.

Fig. 4 is a view showing a configuration of the PLL circuit according to the second embodiment of the present invention.

The PLL circuit of this second embodiment is constructed as a circuit having the following features. More specifically,